Remarks

The present amendment responds to the Official Action dated October 9, 2009. A petition for a one month extension of time and authorization to charge our credit card the fee of $130 is enclosed. The Official Action rejected claims 1-7, 9-12, and 28-30 under 35 U.S.C. § 112, first paragraph. Claims 1-7, 9-12, and 28-30 were also rejected under 35 U.S.C. § 112, second paragraph.

Claims 1-7, 9-11, and 28-30 have been canceled without prejudice. Claims 8, 13-19, and 20-27 have been previously canceled without prejudice. Claim 12 has been amended to be more clear and distinct and new claims 31-49 have been added. Claims 12 and 31-49 are presently pending.

Section 112 Rejections

The Official Action rejected claims 1-7, 9-12, and 28-30 under 35 U.S.C. § 112, first paragraph. The Official Action also rejected claims 1-7, 9-12, and 28-30 under 35 U.S.C. § 112, second paragraph. While applicants do not acquiesce in that analysis believing the previous claims would be clear to one of ordinary skill in the art, the Examiner's rejection is moot with the cancelation of claims 1-7, 9-11, and 28-30. The amended claim 12 depends from and contains all the limitations of newly added claim 39.

In the interest of furthering prosecution, a copy of the independent claims 31, 39, and 47 with reference numbers included has been included as Attachment A. A review showing support for the claimed elements follows.

Claim 31

A "processor with instruction class controllable pipeline" is shown in Fig. 6 operating to execute an example instruction sequence as shown in Fig. 5 for class one and class two instructions of Fig. 2 and described at page 11, lines 13-17, page 13, lines 14-22 and page 17, line 15 – page 19, line 15.

Support for "an adaptable decode stage that decodes in a first time period an instruction received in an instruction register, stores the decoded instruction in a decode register, and generates an instruction class indication that identifies the decoded instruction as a first class instruction or as a second class instruction" can be found at Figs. 2 and 6. Fig. 2 shows a graph 200 of "worst case critical path length of each instruction's execution logic" with a first class "set 210 of instructions" and a "second class set 220 of instructions" is described at page 11, lines 13-17. Fig. 6 shows a decode stage 635 that is adaptable and decodes in a first time period, such as the fifth MCLK cycle 555, an instruction received from instruction register (IR) 625, stores a decoded instruction in decode register 640 and generates "an instruction classification indication 637 from a classify function of the decode logic" as described at page 16, line 20 – page 17, line 2 and page 18, lines 13-19.

Support for an "adaptable execution stage that executes an identified first class instruction in a first class execution logic circuit or executes an identified second class instruction in a second class execution logic circuit in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time that is less than or equal to a first class time period and the second class execution logic circuit has a worst-case signal propagation

time that is greater than the first class time period and assigned to a second class time period" can be found at Figs. 2 and 6. An adaptable execution stage is shown in Fig. 6 as comprising execute stage 650 and multiplexer 654 that executes an identified first class instruction in execute class 1 logic block 652 or executes an identified second class instruction in execute class 2 logic block 656 as described at page 17, lines 10 – 14. "Instruction timing performance is measured by each instruction's critical path, a measure of the worst-case signal propagation time for the instruction in each pipeline stage" as described at page 6, lines 21-23. For example, the execute class 1 logic block 652 executes instructions belonging to a class 1 "set 210 of instructions which have critical paths below 5 ns", which is a first class time period to complete operations for a first class instruction in the adaptable execution stage as described at page 11, lines 13-16. The execute class 2 logic block 656 executes instructions assigned to a class 2 "set 220 of instructions which have critical paths above 5 ns but below 10 ns" which is a second class time period as described at page 11, 13-17.

Support for "an adaptable pipeline control unit responsive to the instruction class indication for an identified second class instruction to select the second class execution logic circuit and to hold the decoded instruction in the decode register until the first time period plus a second time period is equal to the second class time period, wherein stages of the class controllable pipeline advance at a rate that allows the identified second class instruction to complete operations in the adaptable execution stage" can be found at Figs. 5 and 6. An adaptable pipeline control unit is shown as the program flow and pipeline control logic 610 which receives the instruction classification indication 637 from the decode stage 635 as described at page 16,

lines 20-22. In response to a second class instruction indication multiplexer 654 selects the execute class 2 logic block 656 and a hold decode register signal 639 is asserted to hold the decoded instruction in the decode register as described at page 16, line 20 – page 17, line 2. The decoded instruction is generated during first time period as described at page 18, lines 13-19 and line 23 – page 19, line 1. For example with regard to Fig. 5, during "the fifth MCLK cycle 555, ...instruction D(2) 557 is being decoded and classified as a class 2 instruction" as described at page 18, lines 13 and 14. Also, "at the end of the fifth MCLK cycle 555, the decoded and classified instruction D(2) is loaded into the DR 640" as described at page 18, lines 17 and 18. Further, "the decoded and classified instruction D(2) is maintained in the DR 640 by hold DR signal 561, 639" as described at page 18, line 23 – page 19, line 1. As shown in Fig. 5, the hold decode register signal is asserted a second time period shown as a "one-cycle hold of the pipeline" as described at page 17, lines 9 and 10. In this manner, the decoded instruction is held in the decode register until the first time period, such as the fifth MCLK cycle 555 of Fig. 5, plus a second time period, such as the one-cycle hold, is equal to the second class time period as described at page 15, lines 11-14. The class controllable pipeline advances at a rate that allows the identified second class instruction to complete operations in the adaptable execution stage as described at page 15, lines 14 and 15 and page 19, lines 10-12.

Claim 39

A "processor with instruction class controllable pipeline" is shown in Fig. 10 operating to execute an example instruction sequence as shown in Fig. 9B with instructions having an

instruction format as shown in Fig. 9A for instructions classified as shown in Fig. 3, as described at page 11, line 21 – page 12, line 3 and page 25, line 6 – page 28, line 22.

Support for "an adaptable decode stage that decodes an instruction received from an instruction register, stores the decoded instruction in a decode register, and generates an instruction class indication that identifies the decoded instruction as a first class instruction or as a second class instruction" can be found at Figs. 3, 9A, 9B, and 10. Fig. 3 shows a graph 300 having first class instructions 310 and second class instructions 330 as described at page 11, line 21 – page 12, line 1. Fig. 10 shows a decode stage which begins from instruction register (IR) 1010 through decode to decode register (DR) 1012. The decode stage is adaptable and decodes an instruction received from instruction register (IR) 1010, stores a decoded instruction in decode register 1012 and generates an instruction classification indication 1020 from a classify function of the decode logic as described at page 16, lines 20 – 22 that identifies the decoded instruction as a first class instruction, from the set of first class instructions 310, or as a second class instruction from the set of second class instructions 330.

Support for an "adaptable execution stage that executes an identified first class instruction in a first class execution logic circuit or executes an identified second class instruction in a second class execution logic circuit in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time that is less than or equal to a first class time period and the second class execution logic circuit has a worst-case signal propagation time that is greater than the first class time period" can be found at Figs. 3, 9A, and 10. An adaptable execution stage is shown in Fig. 10 as comprising "three classes of execution units 1002,

1004, and 1006" and multiplexer 1024 that executes an identified first class instruction in execute class 1 unit 1002 or executes an identified second class instruction in execute class 2 unit 1004 as described at page 26, lines 10 – 13, page 28, lines 1 and 2 and lines 7 and 8. "Instruction timing performance is measured by each instruction's critical path, a measure of the worst-case signal propagation time for the instruction in each pipeline stage" as described at page 6, lines 21-23. For example, the execute class 1 unit 1002 executes instructions belonging to a class 1 "set 310 of instructions which have critical paths below 5 ns", as described at page 11, lines 21-23. The 5 ns mark is a first class time period. For example, Fig. 9A shows an "instruction classification specified in graph 300 of Fig. 3, a 600 Mhz MCLK is chosen which has a period of ~1.67ns and therefore three MCLK cycles are required for the 5ns class 1 instructions 310 encoding 906", as described at page 25, lines 8-10. The execute class 2 unit 1004 executes "class 2 instructions 330 with an execution logic latency greater than 5ns", as described at page 11, line 23 – page 12, line 1. For example, Fig. 9A shows an encoding 908 for class 2 instructions, as described at page 25, line 11.

Support for "an adaptable pipeline control unit responsive to the instruction class indication for an identified second class instruction to select the second class execution logic circuit and to adjust a period of an adaptable period pipeline clock to allow time for the identified second class instruction to complete operations in the adaptable execution stage" can be found at Figs. 9B and 10. An adaptable pipeline control unit is shown as the program flow and pipeline control logic block in Fig. 10 which receives the classify signal 1020 from decode logic as described at page 26, lines 19 and 20. In response to a second class instruction indication

multiplexer 1024 selects the execute class 2 unit 1004, as described at page 27, lines 3-6. An adaptable period pipeline clock is adjusted as shown in Fig. 9B where a "PCLK column 927 representing adaptable period PCLK cycles" in PCLK cycle 3 943 having three MCLK cycles 947-949, in PCLK cycle 4 950 having four MCLK cycles 954-957, and in PCLK cycle 5 958 having six MCLK cycles 962-967, as described at page 26, lines 2-4. In Fig. 10, the "adaptable clocks, PCLK 1014, PCLK' 1016, and PCLK'' 1019 are logic gated versions of the master clock (MCLK) 1022" and in "some implementations, PCLK 1014, PCLK' 1016, and PCLK'' 1019 may be the same gated clock signal", as described at page 26, line 20 – page 27, line 3. The period of the adaptable period pipeline clock is adjusted to allow time for the identified second class instruction to complete operations in the adaptable execution stage. For example, in Fig. 9B, "[d]uring the next PCLK, PCLK cycle 4 950, ... the pipeline advances at a class 2 four MCLK rate such that by the end of the fourth PCLK cycle 950, ... the decoded and classified instruction C(3) is loaded into the DR 1012, and the instruction B(2) 953 completes its execution in execute class 2 unit 1004 in four elapsed MCLK cycles 954-957", as described at page 28, lines 3-8.

Claim 47

A "processor with instruction class controllable pipeline" is shown in Fig. 10 operating to execute an example instruction sequence as shown in Fig. 9B with instructions having an instruction format as shown in Fig. 9A for instructions classified as shown in Fig. 3, as described at page 11, line 21 – page 12, line 3 and page 25, line 6 – page 28, line 22.

Support for "an adaptable decode stage that decodes an instruction received from an instruction register, stores the decoded instruction in a decode register, and generates an instruction class indication that identifies the decoded instruction as a first class instruction or as a second class instruction" can be found at Figs. 3, 9A, 9B, and 10. Fig. 3 shows a graph 300 having first class instructions 310 and second class instructions 330 as described at page 11, line 21 – page 12, line 1. Fig. 10 shows a decode stage which begins from instruction register (IR) 1010 through decode to decode register (DR) 1012. The decode stage is adaptable and decodes an instruction received from instruction register (IR) 1010, stores a decoded instruction in decode register 1012 and generates an instruction classification indication 1020 from a classify function of the decode logic as described at page 16, lines 20 – 22 that identifies the decoded instruction as a first class instruction, from the set of first class instructions 310, or as a second class instruction from the set of second class instructions 330.

Support for an "adaptable execution stage that executes an identified first class instruction in a first class execution logic circuit or executes an identified second class instruction in a second class execution logic circuit in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time that is less than or equal to a first class time period and the second class execution logic circuit has a worst-case signal propagation time that is greater than the first class time period and assigned to a second class time period" can be found at Figs. 3, 10, and 11. An adaptable execution stage is shown in Figs. 10 and 11 as comprising "three classes of execution units 1002, 1004, and 1006" and multiplexer 1024 that executes an identified first class instruction in execute class 1 unit 1002 or executes an identified

second class instruction in execute class 2 unit 1004 as described at page 26, lines 10 – 13, page 28, lines 1 and 2 and lines 7 and 8. "Instruction timing performance is measured by each instruction's critical path, a measure of the worst-case signal propagation time for the instruction in each pipeline stage" as described at page 6, lines 21-23. For example, the execute class 1 unit 1002 executes instructions belonging to a class 1 "set 310 of instructions which have critical paths below 5 ns", as described at page 11, lines 21-23. The 5 ns mark is a first class time period. The execute class 2 unit 1004 executes instructions assigned to "class 2 instructions 330 with an execution logic latency greater than 5 ns", as described at page 11, line 23 – page 12, line which is the claimed second class time period.

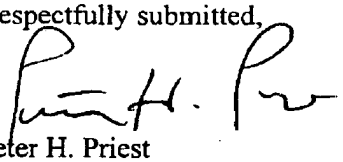
Support for "an adaptable pipeline control unit responsive to the instruction class indication for an identified second class instruction to select the second class execution logic circuit and to adjust a period of an adaptable period pipeline clock to allow time for the identified second class instruction to complete operations in the adaptable execution stage, wherein the adaptable execution stage is synthesized by a single pass synthesis methodology with the period of the adaptable period pipeline clock set to the second class time period during synthesis" can be found at Figs. 9A, 9B, and 10-12. An adaptable pipeline control unit is shown as the program flow and pipeline control logic block in Fig. 10 which receives the classify signal 1020 from decode logic as described at page 26, lines 19 and 20. In response to a second class instruction indication multiplexer 1024 selects the execute class 2 unit 1004, as described at page 27, lines 3-6. A period of an adaptable period pipeline clock is adjusted as shown in Fig. 9B where a "PCLK column 927 representing adaptable period PCLK cycles", as described at page 26, lines 2-4. In Fig. 9B, PCLK

cycle 3 943 comprises three MCLK cycles 947-949, PCLK cycle 4 950 comprises four MCLK cycles 954-957, and PCLK cycle 5 958 comprises six MCLK cycles 962-967. In Fig. 10, the "adaptable clocks, PCLK 1014, PCLK' 1016, and PCLK'' 1019 are logic gated versions of the master clock (MCLK) 1022" and in "some implementations, PCLK 1014, PCLK' 1016, and PCLK'' 1019 may be the same gated clock signal", as described at page 26, line 20 – page 27, line 3. The period of the adaptable period pipeline clock is adjusted to allow time for the identified second class instruction to complete operations in the adaptable execution stage. For example, in Fig. 9B, "[d]uring the next PCLK, PCLK cycle 4 950, ... the pipeline advances at a class 2 four MCLK rate such that by the end of the fourth PCLK cycle 950, ... the decoded and classified instruction C(3) is loaded into the DR 1012, and the instruction B(2) 953 completes its execution in execute class 2 unit 1004 in four elapsed MCLK cycles 954-957", as described at page 28, lines 3-8. The adaptable execution stage is synthesized by a single pass synthesis methodology as described at page 29, line 12 – page 32, line 3 with regard to Figs. 11 and 12. During synthesis, the period of the adaptable period pipeline clock is set to the second class time period as described at page 31, lines 22 and 23

Conclusion

In light of the amendments and new claims contained herein, Applicants submit that the application is in condition for allowance, for which early action is requested. If the Examiner feels the application is not in condition for allowance, the Examiner is invited to call the Attorney below to discuss any steps the Examiner feels is necessary to put the case in condition for allowance.

Respectfully submitted,



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Attachment A

31. (new) A processor with an instruction class controllable pipeline (Figs. 2, 5, and 6) comprising:

an adaptable decode stage (Fig. 6, 635) that decodes in a first time period (Fig. 5, 555) an instruction received from an instruction register (625), stores the decoded instruction in a decode register (640), and generates an instruction class indication (637) that identifies the decoded instruction as a first class instruction (Fig. 2, 210) or as a second class instruction (220);

an adaptable execution stage (650, 654) that executes an identified first class instruction in a first class execution logic circuit (652) or executes an identified second class instruction in a second class execution logic circuit (656) in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time (pg. 6, lines 21-23) that is less than or equal to a first class time period (pg. 11, lines 13-16) and the second class execution logic circuit has a worst-case signal propagation time (pg. 6, lines 21-23) that is greater than the first class time period and assigned to a second class time period (pg. 11, lines 13-17); and

an adaptable pipeline control unit (610) responsive to the instruction class indication for an identified second class instruction to select (654) the second class execution logic circuit and to hold (639) the decoded instruction in the decode register (pg. 16, line 20 – pg. 17, line 2 and pg. 18, line 23 – pg. 19, line 1) until the first time period (555) plus a second time period (559, pg. 17, lines 9 and 10 and pg. 18, lines 19 and 20) is equal to the second class time period (pg. 15, lines 11-14), wherein stages of the class controllable pipeline advance at a rate that allows the

identified second class instruction to complete operations in the adaptable execution stage (pg. 15, lines 14 and 15 and pg. 19, lines 10-12).

39. (new) A processor with an instruction class controllable pipeline (Figs. 3, 9A, 9B, and 10) comprising:

an adaptable decode stage (from instruction register (IR) 1010 through decode to decode register (DR) 1012) that decodes an instruction received from an instruction register (1010), stores the decoded instruction in a decode register (1012), and generates an instruction class indication (1020) that identifies the decoded instruction as a first class instruction (Fig. 3, 310) or as a second class instruction (330);

an adaptable execution stage (1002, 1004, and 1024) that executes an identified first class instruction in a first class execution logic circuit (1002) or executes an identified second class instruction in a second class execution logic circuit (1004) in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time (pg. 6, lines 21-23) that is less than or equal to a first class time period (pg. 11, lines 21-23) and the second class execution logic circuit has a worst-case signal propagation time (pg. 6, lines 21-23) that is greater than the first class time period; and

an adaptable pipeline control unit (Figs. 9B and 10, block labeled "Program Flow & Pipeline Control Logic") responsive to the instruction class indication for an identified second class instruction to select (1024) the second class execution logic circuit and to adjust a period (pg. 26, lines 2- 4) of an adaptable period pipeline clock (Fig. 9B, 927 and Fig. 10, 1014, 1016,

and 1019 and pg. 26, line 20 – pg. 27, line 6) to allow time for the identified second class instruction to complete operations in the adaptable execution stage (pg. 28, lines 3-8).

47. (new) A processor with an instruction class controllable pipeline (Figs. 3, 9A, 9B, and 10) comprising:

an adaptable decode stage (from instruction register (IR) 1010 through decode to decode register (DR) 1012) that decodes an instruction received from an instruction register (1010), stores the decoded instruction in a decode register (1012), and generates an instruction class indication (1020) that identifies the decoded instruction as a first class instruction (Fig. 3, 310) or as a second class instruction (330);

an adaptable execution stage (Fig. 10, 1002, 1004, and 1024 and Fig. 11, 1100) that executes an identified first class instruction in a first class execution logic circuit (1002) or executes an identified second class instruction in a second class execution logic circuit (1004) in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time (pg. 6, lines 21-23) that is less than or equal to a first class time period (pg. 11, lines 21-23) and the second class execution logic circuit has a worst-case signal propagation time (pg. 6, lines 21-23) that is greater than the first class time period and assigned to a second class time period (pg. 11, line 23 – pg. 12, line 1); and

an adaptable pipeline control unit (Figs. 9B and 10, block labeled "Program Flow & Pipeline Control Logic") responsive to the instruction class indication for an identified second class instruction to select (1024) the second class execution logic circuit and to adjust a period

(pg. 26, lines 2- 4) of an adaptable period pipeline clock (Fig. 9B, 927 and Fig. 10, 1014, 1016, and 1019 and pg. 26, line 20 – pg. 27, line 6) to allow time for the identified second class instruction to complete operations in the adaptable execution stage (pg. 28, lines 3-8), wherein the adaptable execution stage (Fig. 11, 1100) is synthesized by a single pass synthesis methodology (Fig. 12, 1200) with the period of the adaptable period pipeline clock set to the second class time period during synthesis (1240).